Texas A&M University–Corpus Christi
College of Science and Technology
Engineering Technology

ENTC 3416 Digital Logic
Spring 2006

COURSE INFORMATION

Meeting Time: (Lecture) TR 5:30 p.m. – 6:45 p.m. (Laboratory) TR 7 p.m. – 8:15 p.m.
Meeting Place: ST 220 (Lecture), ST 220 (Laboratory)

PROFESSOR INFORMATION

Dr. Ruby Mehrubeoglu
Office Address: Room ST 222B
Office Phone: (361) 825-3378
E-mail Address: ruby.mehrubeoglu@tamucc.edu
Web Page Address: http://www.sci.tamucc.edu/~entc/RubyPage.html
Office Hours: TR 2:00 p.m. –5:00 pm, and by appointment

COURSE DESCRIPTION

This course introduces the principles of digital logic analysis and design. Topics include logic gates, number systems and conversions, Boolean algebra, logic simplification, combinational circuits, programmable logic devices, and sequential circuits. The laboratory provides hands-on experience with devices and circuits discussed in the classroom. A software program, Electronics Workbench, is used for circuit analysis and simulation.

PREREQUISITES

ENTC 2414 Circuit Analysis I

TEXTS AND OTHER SUPPLIES

1. Digital Fundamentals, Thomas Floyd, 8th Edition, 2003, Prentice Hall.
2. Experiments in Digital Fundamentals, David Buchla, 6th Edition, 2003, Prentice Hall.

COURSE OUTCOMES

This course is designed to enable students to:

- Convert between decimal, binary, octal and hexadecimal numbers
- Perform addition and subtraction in the four bases studied (10, 2, 8, and 16) and use various codes, ex. ASCII, gray code, BCD, etc.
- Apply the basic laws and rules of Boolean algebra
- Simplify Boolean expressions using the laws and rules of Boolean algebra and/or a Karnaugh map
- Convert any Boolean expression into a sum-of-products (SOP) or product-of-sums (POS)
- Analyze combinational logic circuits and write their Boolean output expressions
- Design a combinational logic circuit for a given Boolean expression or truth table
- Simplify a combinational logic circuit to its minimum form

- Use a wide range of digital chips, from simple AND, OR, NOT, NAND and NOR gates to adders, subtractors, decoders, and multiplexers
- Use PALs and GALs to implement combinational logic functions
- Identify and analyze basic flip-flops types (D, T, S-R and J-K) and clocking variations (edge-triggered, master-slave, and transparent)
- Wire a 555 timer to operate as either an astable multivibrator or a one-shot
- Describe the difference between synchronous and asynchronous counters
- Analyze and design counter and shift register circuits
- Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate
- Describe the characteristics of RAM, ROM, PROM, and flash memories
- Show how to expand ROMs and RAMs to increase length and word capacity
- Describe an FPGA and explain how it differs from a CPLD
- Interpret timing diagrams of digital circuits
- Explain how propagation delay affects the speed of a circuit
- State basic differences between TTL and CMOS
- Use data sheets to obtain information about gates and devices
- Calculate the power dissipation of a device and explain what fan-out of a gate means
- Connect circuits in a wired-AND configuration
- Describe the operation of tristate circuits
- Build, test, and troubleshoot digital circuits
- Use a software package to analyze and design digital circuits.

INSTRUCTIONAL METHODS AND ACTIVITIES

Methods and activities for instruction include the following: lectures, group discussions, homework assignments/solutions, lab experiments/exercises, and software simulation.

EVALUATION AND GRADE ASSIGNMENT

Evaluation of student performance is based on homework assignments, a quiz, two midterms, lab experiments/exercises, and a final exam. Tests are graded within a week from the date they are taken. No makeup exams are given in this course. The final grade is assigned as follows.

	Points		**If**	**Grade**
Quiz	05		90 ≤ Total	A
Midterm 1	25		80 ≤ Total < 90	B
Midterm 2	25		70 ≤ Total < 80	C
Lab experiments/reports	10		60 ≤ Total < 70	D
Homework	5		Total < 60	F
Final	30			
Total	100			

SAFETY

The safety of students, faculty, staff and visitors to the ET laboratories is of paramount importance to the ET programs. You must follow safety procedures and use personal protective equipment as required in each laboratory. Any student that attempts to use equipment without authorization or that violates any safety policy or regulation will be immediately removed from the laboratory.

FOOD AND DRINKS
Eating and/or drinking is permitted ONLY in designated areas.

TENTATIVE WEEKLY SCHEDULE*

WK	Week of	Readings	Topics	Exams
1	1/09	Ch. 1	Digital concepts	
2	1/16	Ch. 2	Number systems and codes	
3	1/23	Ch. 3	Logic gates	
4	1/30	Ch. 4	Boolean algebra	QUIZ
5	2/06	Ch. 4	Logic simplification	
6	2/13	Ch. 5	Combinational logic	MID 1
7	2/20	Ch. 5	NAND and NOR circuits	
8	2/27	Ch. 6	Functions of combinational logic	
9	3/06	Ch. 6	Functions of combinational logic	
10	3/13	**S P R I N G B R E A K**		
11	3/20	Ch. 7	PLD arrays and classifications	
12	3/27	Ch. 7	PALs and GALs	MID 2
13	4/03	Ch. 8	Flip-flops, one-shots, timers	
14	4/10	Ch. 9	Counters	
15	4/17	Ch. 10	Shift registers	
16	4/24	Ch. 12	Memory	
17	5/01	Ch. 15	Integrated circuit technologies	
17	Date: Thursday, May 04, 2006. Time: 4:30-7:00 p.m.			FINAL

*****Changes to the weekly schedule will be announced in class

TENTATIVE LABORATORY SCHEDULE

EXP. #	TITLE
1	Lab Instruments
2	Constructing a Logic Probe
3	Number Systems
4	Logic Gates
7	Boolean Laws & DeMorgan's Theorem
8	Logic Circuit Simplification
9	The Perfect Pencil Machine –Design
9	The Perfect Pencil Machine - Build and Demo
11	Adder and Magnitude Comparator
12	Combinational Logic Using Multiplexers
13	Combinational Logic Using Demultiplexers
15	The D Latch and D Flip-Flop
17	The J-K Flip-Flops
18	One-Shots and Astable Multivibrators

SUPPORT SERVICES FOR STUDENTS WITH DISABILITY
Refer to the University Catalog.

ATTENDANCE POLICY
You are advised to attend all lectures and laboratory sessions. If you miss a class period, you are responsible for whatever was covered/announced during your absence.

ACADEMIC HONESTY
Your attention is called to the University policy in the Student Handbook.

ASSIGNMENTS
Late assignments are not normally accepted. The student will receive a zero on assignments that are turned in after the due date unless a written permission (by email) is secured (from the instructor) prior to the due date. Permission will be granted only in extreme situations. Assignments may be turned in before the due date (they may be left in my mailbox, sent with a classmate, mailed, etc.).

LAB EXPERIMENTS
The goal of the laboratory sessions is to analyze and verify the theoretical ideas learned in the classroom. All theoretical analysis and data calculations must be done before the lab – this makes performing the experiments run much smoother.

LAB REPORTS
Students must submit a written report a week after each experiment is performed. You will not receive credit for any late reports unless you secure a written permission (by email) from the instructor prior to the due date. Reports may be turned in before the due date. Guidelines for lab reports will be distributed in class.

EMAIL ADDRESS
You must supply the instructor with a current email address and check your email account daily. You supply your email address by sending an email message by the end of the first week to ruby.mehrubeoglu@tamucc.edu. In the subject area, type ENTC 3416.

SUPPLEMENTARY READING LIST
1. Fundamentals of Logic Design, 5th Ed.,C. Roth, Jr., Thomson-Brooks/Cole, 2004
2. Fundamentals of Digital Logic and Microcomputer Design, M. Rafiquzzaman, Rafi Systems, Inc., 2003
3. Digital Electronics with PLD Integration, N. Cook, Prentice Hall, 2001
4. Digital Design with CPLD Applications and VHDL, Dueck, Delmar, 2001
5. Digital Systems: Principles and Applications, Tocci, Prentice Hall, 1999
6. Logic and Computer Logic Design Fundamentals, Mano & Kime, Prentice Hall, 1997
7. Digital Integrated Circuits, Rabaey, Prentice Hall, 1996
8. Practical Digital Design Using ICs, Greenfield, Prentice Hall, 1994
9. Fundamentals of Digital Electronics, West, Dueck, 1994
10. Introduction to Digital Technology, Nashelsky, Prentice Hall, 1994
11. Digital Electronics, Bignell and Donovan, Delmar, 1994

NOTE: Most of these books are available in the University library.