Texas A&M University–Corpus Christi
College of Science and Technology
Engineering Technology

ENTC 4496 Directed Independent Study
Digital Logic
Fall 2007

COURSE INFORMATION

Meeting Time: T 2:00 – 3:00 pm. W: 10:00 – 11:00 am.
Meeting Place: ST 222B
Lab: ST 220, buddy system (only with another student)

PROFESSOR INFORMATION

Dr. Ruby Mehrubeoglu
Office Address: Room ST 222B
Office Phone: (361) 825-3378
E-mail Address: ruby.mehrubeoglu@tamucc.edu
Office Hours: T 2:00 p.m. –5:00 pm, W 10:00 – 12:00 and by appointment

COURSE DESCRIPTION

Introduces the principles of digital logic analysis and design: logic functions, logic gates, binary, octal, hexadecimal systems and number conversions; boolean algebra; algebraic simplifications; combinational and sequential logic, and use of simulation software, PLCs.

PREREQUISITES

ENTC 2414 Circuit Analysis I

TEXTS AND OTHER SUPPLIES

1. Digital Fundamentals, Thomas Floyd, 8th Edition, 2003, Prentice Hall.
2. Experiments in Digital Fundamentals, David Buchla, 6th Edition, 2003, Prentice Hall.

COURSE OUTCOMES

This course is designed to enable students to:

- Understand number conversions, and convert between multiple number systems (decimal, binary, octal, hexadecimal
- Perform arithmetic in multiple number systems
- Apply Boolean Algebra and Karnaugh maps to simplify Boolean expressions
- Convert any Boolean expression into a sum-of-products (SOP) or product-of-sums (POS)
- Write their Boolean output expressions
- Design and analyze combinational logic circuit
- Simplify logic circuits
- Implement and test logic gates such as AND, OR, NOT, NAND and NOR
- Use PALs and GALs to implement combinational logic functions
- Analyze basic flip-flops types (D, T, S-R and J-K) and clocking variations (edge-

triggered, master-slave, and transparent)
- Wire a 555 timer to operate as either an astable multivibrator or a one-shot
- Analyze and design counter and shift register circuits
- Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate
- Show how to expand ROMs and RAMs to increase length and word capacity
- Describe an FPGA and explain how it differs from a CPLD
- Interpret timing diagrams of digital circuits
- Analyze effects of propagation delay on the speed of a circuit
- Identify differences between TTL and CMOS circuitry
- Be able to use data sheets on gates and other logic devices
- Calculate the power dissipation of a device and explain what fan-out of a gate means
- Use a software package to analyze and design digital circuits.

INSTRUCTIONAL METHODS AND ACTIVITIES
Methods and activities for instruction include the following: lectures, group discussions, homework assignments/solutions, lab experiments/exercises, and software simulation.

EVALUATION AND GRADE ASSIGNMENT
Evaluation of student performance is based on homework assignments, a quiz, two midterms, lab experiments/exercises, and a final exam. Tests are graded within a week from the date they are taken. No makeup exams are given in this course. The final grade is assigned as follows.

	Points		**If**	**Grade**
Weekly Meetings	5		$90 \leq$ Total	A
Midterm 1	20		$80 \leq$ Total < 90	B
Midterm 2	20		$70 \leq$ Total < 80	C
Lab experiments/reports	15		$60 \leq$ Total < 70	D
Homework	10		Total < 60	F
Lab Notebook	5			
Final	25			
Total	100			

SAFETY
The safety of students, faculty, staff and visitors to the ET laboratories is of paramount importance to the ET programs. You must follow safety procedures and use personal protective equipment as required in each laboratory. Any student that attempts to use equipment without authorization or that violates any safety policy or regulation will be immediately removed from the laboratory.

FOOD AND DRINKS
Eating and/or drinking is permitted ONLY in designated areas.

WEEKLY SCHEDULE

WK	Readings	Topics	Exams
1	Ch. 1	Digital concepts	
2	Ch. 2	Number systems	
3	Ch. 3	Simple logic gates	
4	Ch. 4	Boolean algebra	
5	Ch. 4	Logic simplification	
6	Ch. 5	Combinational logic	MID 1
7	Ch. 5	NAND and NOR circuits	
8	Ch. 6	Functions of combinational logic	
9	Ch. 6	Functions of combinational logic	
10	Ch. 11	PLD arrays and classifications	
11	Ch. 11	PALs and GALs	
12	Ch. 7	Flip-flops, one-shots, timers	MID 2
13	Ch. 8	Counters	
14	Ch. 9	Shift registers	
15	Ch. 10	Memory	
16	Ch. 14	Integrated circuit technologies	

LABORATORY SCHEDULE

EXP. #	TITLE
1	Lab Instruments
2	Constructing a Logic Probe
3	Number Systems
4	Logic Gates
7	Boolean Laws & DeMorgan's Theorem
8	Logic Circuit Simplification
9	The Perfect Pencil Machine –Design
9	The Perfect Pencil Machine - Build and Demo
11	Adder and Magnitude Comparator
12	Combinational Logic Using Multiplexers
13	Combinational Logic Using Demultiplexers
15	The D Latch and D Flip-Flop
17	The J-K Flip-Flops
18	One-Shots and Astable Multivibrators

SUPPORT SERVICES FOR STUDENTS WITH DISABILITY
Refer to the University Catalog.

ATTENDANCE POLICY
You are advised to attend all lectures and laboratory sessions. If you miss a class period, you are responsible for whatever was covered/announced during your absence.

ACADEMIC HONESTY
Your attention is called to the University policy in the Student Handbook.

ASSIGNMENTS
Late assignments are not normally accepted. The student will receive a zero on assignments that are turned in after the due date unless a written permission (by email) is secured (from the instructor) prior to the due date. Permission will be granted only in extreme situations. Assignments may be turned in before the due date (they may be left in my mailbox, sent with a classmate, mailed, etc.).

LAB EXPERIMENTS
The goal of the laboratory sessions is to analyze and verify the theoretical ideas learned in the classroom. All theoretical analysis and data calculations must be done before the lab – this makes performing the experiments run much smoother.

LAB REPORTS
Student must submit a written report a week after each experiment is performed. You will not receive credit for any late reports unless you secure a written permission (by email) from the instructor prior to the due date. Reports may be turned in before the due date. Guidelines for lab reports will be distributed.